Claims:

1. A method for performing a processing function of a memory in a block memory comprising memory cells, where data can be stored, and a connection bus comprising at least a ready/busy line, which can be set at least to a ready status and to a busy status, said method comprising setting the status of said ready/busy line to said busy status in a beginning of the processing function, performing detection of processing errors, indicating an end of processing function by setting said ready/busy line to said ready status, and changing the status of said ready/busy line back to said busy status if a processing error is detected.

2. The method according to claim 1, wherein erasing the block memory is used as said processing function, the method comprising performing a comparison of an erased memory cell with the data meant for the status of the erased memory cell in connection with erasing, in order to detect erasing errors, and if an erasing error is detected in the comparison, changing the status of said ready/busy line back to said busy status.

3. The method according to claim 1, wherein storing data to the block memory is used as said processing function, the method comprising performing a comparison of stored data with data meant to be stored in connection with storing the data, in order to detect storing errors, and if a storing error is detected in the comparison, changing the status of said ready/busy line back to said busy status.

4. The method according to claim 1, wherein copying data in the block memory from one location to some other location is used as said processing function, the method comprising performing a comparison of copied data with data meant to be copied in connection with copying the data, in order to detect copying errors, and if a copying error is detected in the comparison, changing the status of said ready/busy line back to said busy status.

5. The method according to claim 1, wherein reading data from the block memory is used as said processing function, the method comprising performing examining status of a memory cell being read in connection with reading data, and if a memory cell error is detected in the examination, changing the status of said ready/busy line back to said busy status.

6. The method according to claim 1, comprising starting the processing function by sending a command to the block memory, and setting the status of said ready/busy line to the busy status in a stage when a function according to the command is started in the block memory.

7. The method according to claim 1, wherein the block memory is divided into blocks, and each block is divided into pages, the method comprising transmitting data to the block memory page by page.

8. The method according to claim 7, comprising performing erasing of at least one block, and setting a previously determined status as the status of all the memory cells of said at least one block.

9. The method according to claim 1, comprising examining the status of said ready/busy line, and performing re-examination of the status of the ready/busy line when it changes from the busy status to the ready status.

10. The method according to claim 1, wherein the connection bus comprises a data bus comprising at least one data line, the method comprising using the data line of said data bus as a ready/busy line.

11. A system, which comprises an electronic device comprising a block memory comprising memory cells for storing data, and a connection bus comprising at least a ready/busy line, and at least a ready status and a busy status are defined for said ready/busy line, and which block memory comprises means for changing the status of said ready/busy line to said busy status in the beginning of the

processing function of the block memory, a comparator for detecting processing errors, and means for indicating the end of processing function by setting said ready/busy line to said ready status, the system further comprising means for changing the status of said ready/busy line back to said busy status after detecting a processing error.

12. The system according to claim 11, wherein said processing function is one of the following:

emptying the memory cells,
storing data in memory cells,
copying data between memory cells,
reading the data stored in the memory cells.

13. The system according to claim 11, comprising a processor, and a first connection bus between the processor and the block memory, and means for starting the processing function by sending a command to the block memory, and means for setting the status of said ready/busy line to the busy status when the function according to the command has been started in the block memory.

14. The system according to claim 13, comprising means for creating an interrupt in the processor when the status of the ready/busy line changes from the busy status to the ready status, and the processor comprising means for examining the status of the ready/busy line in connection with handling the interrupt.

15. The system according to claim 11, comprising a processor, a memory controller, a first connection bus between the processor and the memory controller, and a second connection bus between the memory controller and the block memory, in which case the commands are arranged to be sent from the processor to the memory controller, as well as from the memory controller to the block memory, the system comprising means for starting storing of the data by sending a command to the block memory, and means for setting the

status of said ready/busy line to the busy status when the function according to the command has been started in the block memory.

16. The system according to claim 15, comprising means for creating an interrupt in the memory controller when the status of the ready/busy line changes from the busy status to the ready status, wherein the memory controller comprises means for examining the status of the ready/busy line in connection with handling the interrupt, and means for forming an interrupt to the processor if the ready/busy line is in the busy status.

17. The system according to claim 11, wherein the block memory is divided into blocks, and each block is divided into pages, the system comprising means for transmitting data to the block memory page by page.

18. The system according to claim 11, the bus interface comprising a data bus comprising at least one data line, and that the data line of said data bus is arranged to be used as a ready/busy line.

19. An electronic device, which comprises block memory comprising memory cells for storing data, and a bus interface comprising at least a ready/busy line and at least a ready status and a busy status are defined for said ready/busy line, and which block memory comprises means for setting the status of said ready/busy line to said busy status in the beginning of a processing function of the block memory, a comparator for detecting processing errors, and means for indicating an end of the processing function by setting said ready/busy line to said ready status, the electronic device further comprising means for changing the status of said ready/busy line back to said busy status after detecting a processing error.

20. A block memory comprising memory cells for storing data, and a connection bus comprising at least a ready/busy line, and at least a ready status and a busy status are defined for said ready/busy line, and which block memory comprises means for setting the status of

said ready/busy line to said busy status in a beginning of a processing function of the block memory, a comparator for detecting processing errors, and means for indicating an end of processing function by setting said ready/busy line to said ready status, the block memory further comprising means for changing the status of said ready/busy line back to said busy status after detecting a processing error.

21. The memory block according to claim 20, wherein said processing function is one of the following:

emptying the memory cells
storing data in memory cells,
copying data between memory cells,
reading the data stored in the memory cells.

22. The block memory according to claim 20, comprising a comparator for comparing the data stored in the memory cells with data meant to be stored in order to detect storing errors.